



JMGG140V12A

Description

JMG N-channel Advanced Mode Power MOSFET

Features

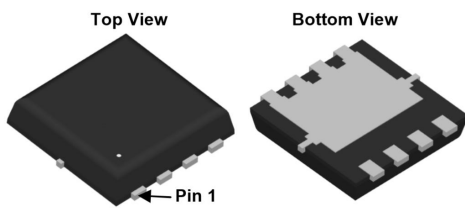
- 120V,50A
 $R_{DS(ON)} < 13.8m\Omega @ V_{GS} = 10V$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Application

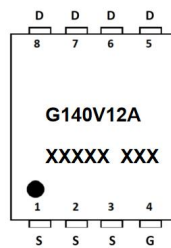
- Load Switch
- PWM Application
- Power Management



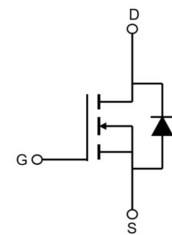
100% UIS TESTED!
100% ΔVds TESTED!



PDFN5x6-8L



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
G140V12A	JMGG140V12A	TAPING	PDFN5x6-8L	13"	2500	25000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	120	V
V_{GSS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	50 A
		$T_C = 100^\circ C$	33 A
I_{DM}	Pulsed Drain Current ^{note1}	200	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	81	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	60 W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	120	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±25V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	-	4	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} =10V, I _D =20A	-	11	13.8	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	1625	-	pF
C _{oss}	Output Capacitance		-	1230	-	pF
C _{rss}	Reverse Transfer Capacitance		-	29	-	pF
Q _g	Total Gate Charge	V _{DD} =60V, I _D =20A, V _{GS} =10V	-	37	-	nC
Q _{gs}	Gate-Source Charge		-	14	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	8	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =20A, R _{GEN} =3Ω, V _{GS} =10V	-	11	-	ns
t _r	Turn-on Rise Time		-	7.5	-	ns
t _{d(off)}	Turn-off Delay Time		-	26	-	ns
t _f	Turn-off Fall Time		-	4	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F =30A, di/dt=100A/μs	-	58	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	149	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: Starting T_J=25°C, V_{DD}=60V, V_{GS}=10V, R_g=25Ω, L=0.5mH, I_{AS}=18A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

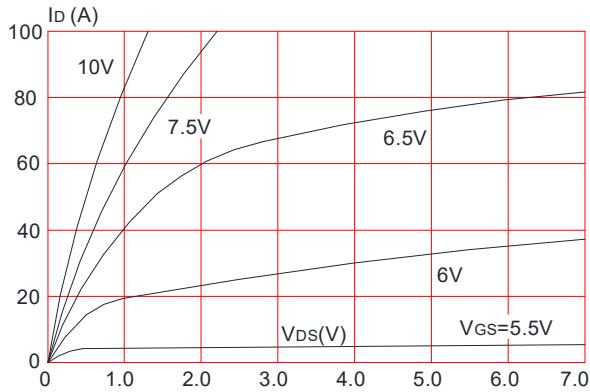


Figure 2: Typical Transfer Characteristics

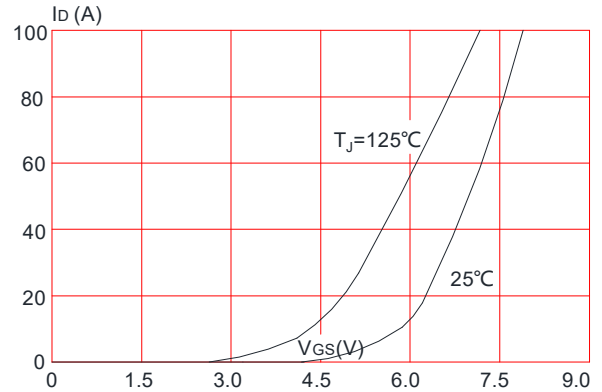


Figure 3: On-resistance vs. Drain Current

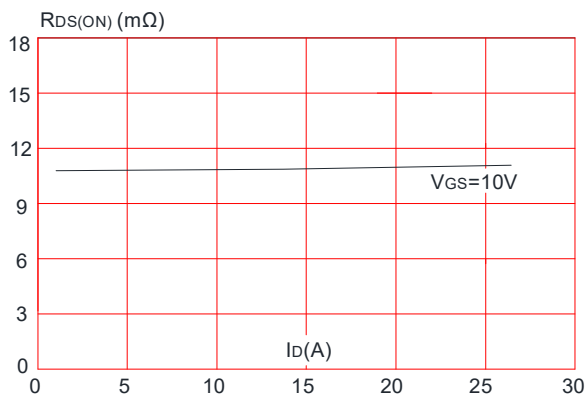


Figure 4: Body Diode Characteristics

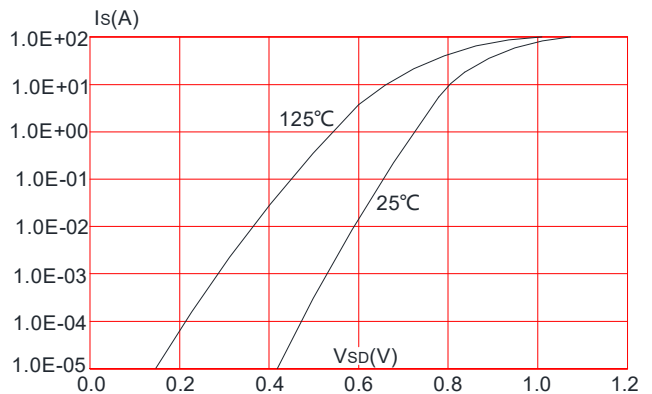


Figure 5: Gate Charge Characteristics

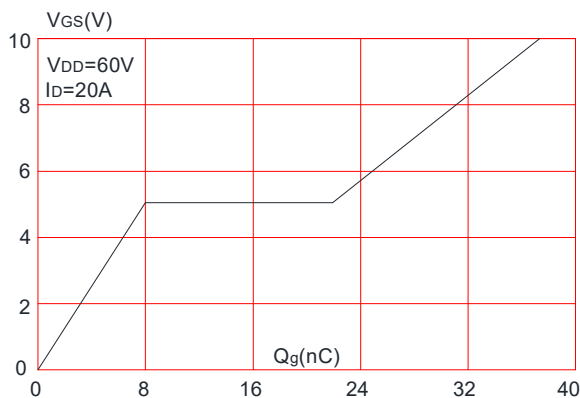


Figure 6: Capacitance Characteristics

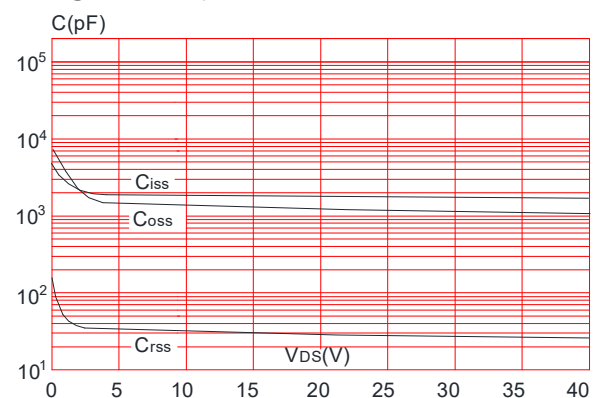




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

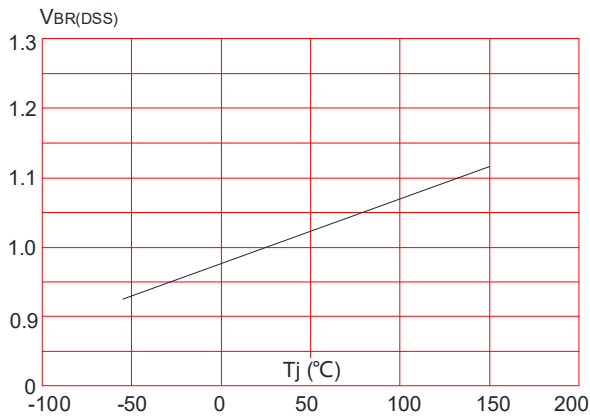


Figure 8: Normalized on Resistance vs. Junction Temperature

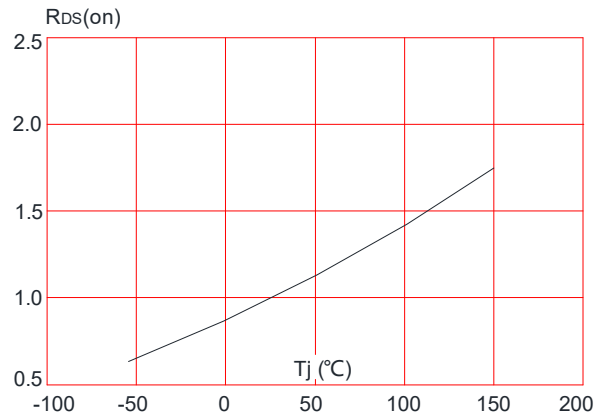


Figure 9: Maximum Safe Operating Area

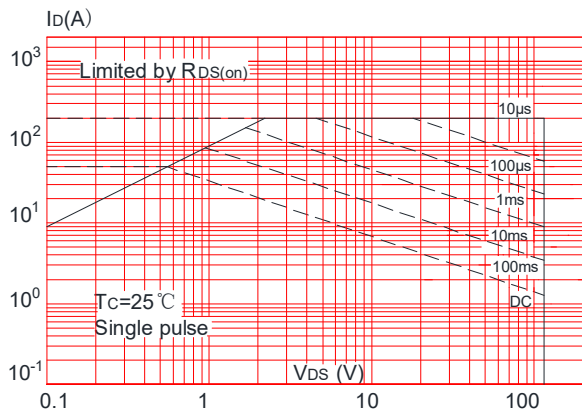


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

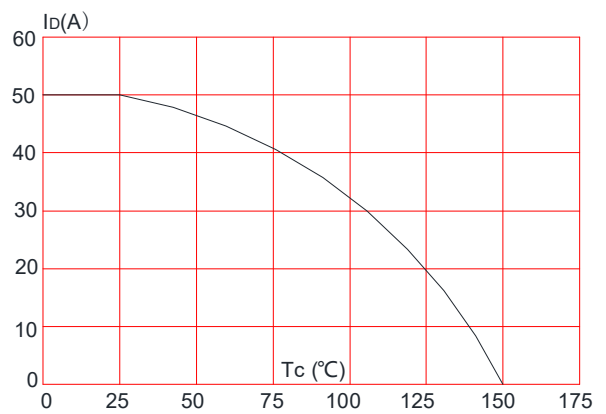
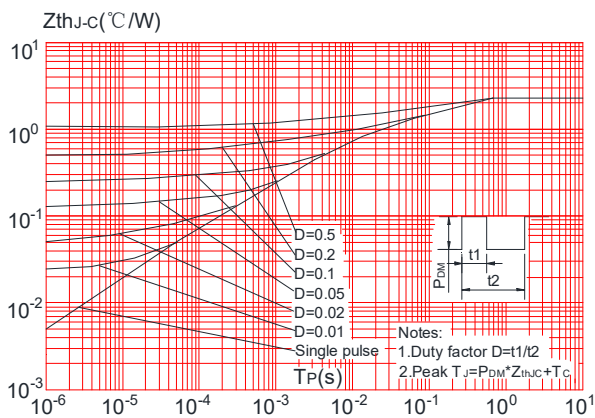


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

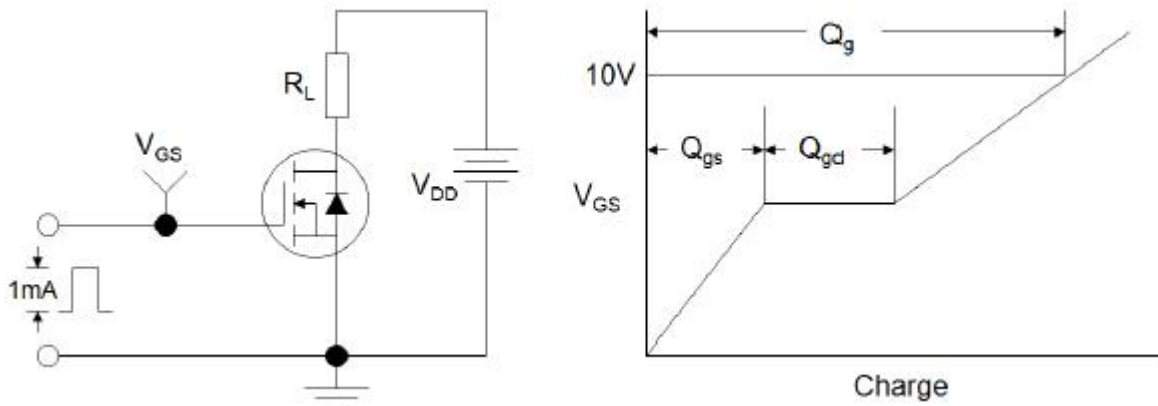


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

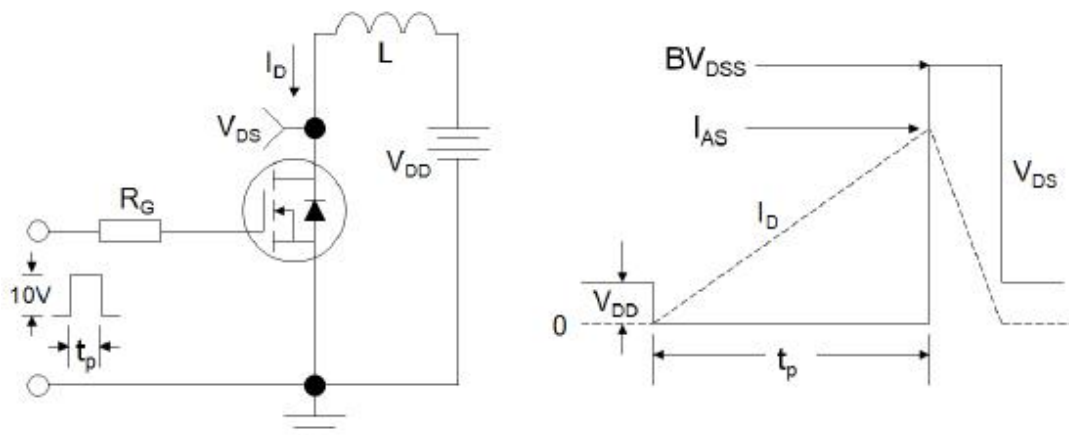
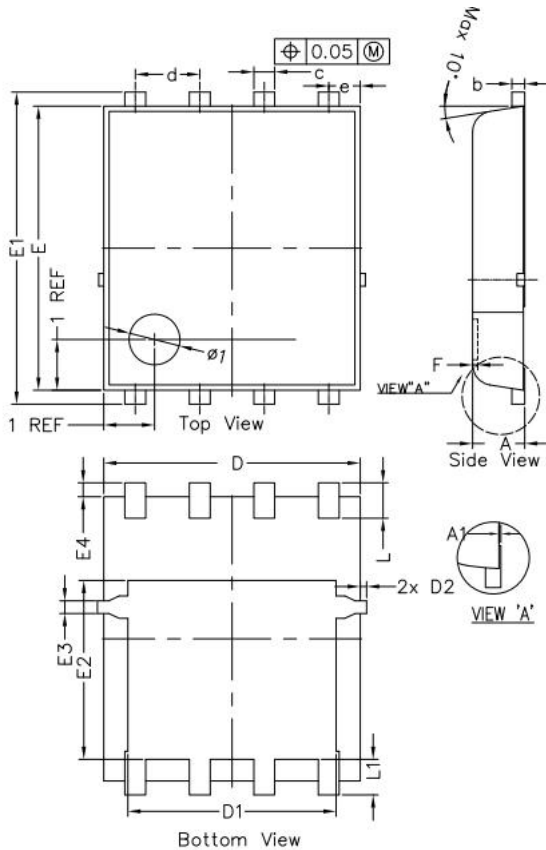


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-PDFN5x6-8L



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	----	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d	1.27 BSC			0.050 BSC		
* D	4.950	5.050	5.150	0.195	0.199	0.203
D1	4.000	4.100	4.200	0.157	0.161	0.165
* D2	---	---	0.125	---	---	0.005
e	0.62 BSC			0.024 BSC		
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.425	3.525	3.625	0.135	0.139	0.143
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
* L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2022 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.